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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,973	09/25/2003	Tuan M. Quach	42P17508	8868

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,973	QUACH ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#1-3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6-9 and 17-24 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. No. 6,407,960 to Egbert et al. (Egbert).

3. Per claim 1, Egbert discloses a method for accessing configuration registers (Fig. 1, EEPROM 14 contains value for configuration registers, element 12), comprising: a) receiving an indication that an attempt has been made to access a first register (after first register, e.g., Fig. 1, element 14 at address 0000, has been read, as long as the MSB is not 0, the next even register address AV2 is read), the first register to reflect an index variable (index variable is the value inside AV1, AV2...Ax, indexing a corresponding configuration register, A1, A2...Ax) that points to a configuration register (AV1 is the address value that points to configuration register A1, Fig. 1, element 12a; Column 3, lines 19-25) and then b) receiving an indication that an attempt has been made to access a second register (again, as long as MSB in the second register AV2 is not 0, an indication is given to keep proceeding until a MSB or 1 is found; this is represented by Fig. 2, element 54, where if MSB is "N", then it is indicates that a second

register is effectively read), the second register to reflect part of the contents of a configuration register to which the index variable points (Fig. 1, element 12, AV2 and D2 reflects the contents of A2, the index variable being the value inside AV2, the address value, that points to A2; and then c) in response to b), and without waiting for another attempt to access the first register, changing the index variable to point to another configuration register (the address values AV, are incremented until MSB is set, without looking waiting from another attempt to access previous registers; Fig. 2).

4. Per claim 2, Egbert discloses claim 1, wherein the attempt to access the first register is an attempt to write a given index value that points to a given configuration register (AV1 is the index pointing to configuration register A1, wherein it allows the writing of an index value D1 to configuration register A1), and wherein the attempt to access the second register is an attempt to write a given content value that is to be part of the content of the given configuration register (second register AV2 points to configuration register A2, to write content value D2 into A2, which can be a continuation of configuration information from D1).

5. Per claims 3 and 4, Egbert discloses claim 2, wherein both the given index and content values (AV and D values) as written to the first and second registers (configuration registers A1, A2...), respectively, is encoded (Fig. 1, element 22 shows the need to decode information from EEPROM, element 14).

6. Per claim 6, Egbert discloses claim 1, wherein in c), the index variable is changed only if a special mode of operation (MSB being set to 1 would change the address value reading, e.g., halting it as shown in Fig. 2, elements 62 and 64), for

programming configuration via automatic indexing (Fig. 1, address values automatically read until MSB being set is encountered), has been entered.

7. Per claim 7, Egbert discloses a method for programming a plurality of configuration registers (Fig. 2), comprising: a) enabling a first mode (first mode here is base on the MSB of each address value in EEPROM being set to 0, if 0 then data value, Dx, will be written to configuration registers, Ax) of operation for an IC component (EEPROM is by definition an IC) in which a plurality of configuration registers (Fig. 1, element 12 are configuration registers are to be programmed (EEPROM, element 14 programs configuration registers) according to b)-e); b) writing to a first control register (AV1) in said IC component to enable access to a selected one of the registers (A1 points to register A1); and then c) writing to a second control register in said IC component a content value (D1 in EEPROM, element 14, is the content for register A1) for said selected one of the registers; and then d) writing to the second control register a further content value for another selected one of the registers, without again writing to the first control register (AV2 is for a second register, A2); and then e) repeating d) until all of the registers have been programmed (various address values in EEPROM, element 14, program configuration registers in element 12, until MSB=1 is encountered).

8. Per claims 8 and 9, Egbert discloses claim 7, further programming a plurality of registers (Fig. 1, EEPROM can have address values up to how much memory the EEPROM can handle), f) disabling the first mode of operation (MSB is set to 1 by operator, Fig. 1, element 26); and then g) writing to the first control register to enable

access to a selected one of the further registers (MSB is set to 0 in other address registers); and then h) writing to the second control register a content value for said selected one of the further registers (D2 is the value for AV2 to be written to A2); and then repeating g)-h) until all of the further registers have been programmed (all the address values program the registers in element 12, until MSB set to 1 is encountered). Note the EEPROM register control addresses are programmed sequentially, i.e., addresses 0000, 0001, 0002, etc.

9. Claims 17-24 are significantly similar to claims 1-4 and 6-9 and therefore the rejections are applied accordingly. Note that Egbert discloses serial bus communication between the EEPROM, element 14, and the configuration registers, element 10, having bus events that trigger reading and writing of register values. Also the IC, element 10 has its control registers, element 12, mapped to the I/O address space, element 14.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Egbert.

Egbert discloses claim 2. Egbert further discloses address values (AVx) and data values (Dx) are programmable (Column 3).

Egbert does not disclose expressly accessing register values more than one time.

At the time of the invention it would have been obvious to a person of ordinary skill in the art that address values can actually point to the same configuration registers. For instance AV2-AV5 may point to the same value as AV1. In this situation, one can quickly list several test register data values and set all address values to point to the same configuration register. One would simply need to set the MSB to 1 to indicate where to stop reading the last value. This way, one can test several configurations quickly, by simply setting the MSB at the data value one wishes to set and resetting the power to see the effect.

The suggestion/motivation for doing so would have been for convenience during testing/test bench of the chipset.

Therefore, it would have been obvious to access certain registers multiple times in order to quickly test various configuration values and see their effects on the devices to which the registers correspond.

12. Claims 10-12 is rejected under 35 USC 103(a) as being unpatentable over Egbert.

Egbert discloses an IC circuit component (Fig. 1, element 10) comprising a plurality of configuration registers (Fig. 1, element 12); having various index values corresponding to sequential addresses (Fig. 1, element 14, addresses 0000, 0001, 0002). Egbert further discloses logic (Fig. 1, element 16) that interfaces the EEPROM, element 14 to read address values (AV) and data (D) to program the configurable registers, which determine modes of operations (MSB=1 then end programming/reading address values). Egbert also discloses detection logic (Fig. 1, element 18) that detects

control signals (Fig. 1, EExx are control signals going between external memory interface and EEPROM) that requests access/programming of configuration registers (Fig. 1, element 12).

Egbert does not disclose expressly counters or multiplexer logic that implement the functionality/methodology of the programming of the registers (the functionality/methodology previously described in the rejection for claim 1).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use multiplexer as the switching logic in the mode of operation to determine what to do in the case MSB=1 or MSB=0 as well as counters to automatically increment the index values.

The suggestion/motivation for doing so would have been that muxes and counters are fundamental digital elements in computer architecture, where the address incrementing in Fig. 1, element 14 would have intrinsically been performed by counters and determining and selecting which mode to operate in would intrinsically be performed by basic switching circuitry such as multiplexers as a matter of design choice.

Therefore, it would have been obvious to use multiplexer and counters since they are basic digital circuitry used pervasively in practice to construct various functional digital blocks.

13. Claims 13-16 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. Greger et al. (Greger).

14. Per claim 13, Greger discloses a first processor (Fig. 1) and main memory combination (Fig. 1, element 150 is main memory subsystem); a graphics subsystem (Fig. 1, element 170); and an I/O hub to bridge the first combination and graphics subsystem (Fig. 1, element 130, system address chip) via I/O ports/links; the I/O hub has a plurality of configuration registers (Fig. 4, element 410 is representative of one of many registers in Fig. 1); the I/O hub having a first index value (Fig. 4, element 402), multiplexor logic operating with index value (Fig. 3, elements 312-316); Greger further discloses various control circuitry/signals required to control input/output from devices outside of the System Address Chip (Figs. 1 and 3, element 130).

Greger does not disclose expressly the user of counters in incrementing and decrementing the index.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use counters to automatically increment/decrement the index values.

The suggestion/motivation for doing so would have been that anytime in digital design that multiple values exist that require the cycling through of those values, counters intrinsically used as a matter of design choice.

Therefore, it would have been obvious to use counters since there are multiple index values required to be cycled through.

15. Per claims 14 and 15, Greger discloses claim 13, further disclosing several more point-to-point connections to other devices that can be made at the I/O hub (Fig. 1, element 130), to external devices (elements 192 and 194) and PCI peripheral devices (Fig. 1, elements 160).

16. Per claim 16, Greger discloses claim 13, wherein the I/O hub has a configuration register that contains a port number (Fig. 5, element 504), function number (Fig. 5, element 514), register number (Fig. 5, element 516).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited (Form PTO-892) attached to this action to further show the state of the art with respect to indexing of programmable registers.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIM HUYNH
SUPERVISORY PATENT EXAMINER
3/20/06